

DPW

Attorney's Docket No. 42P15685  
Confirmation No.: 6439

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:

Scott A. Hareland, et al.

Application No.: 10/607,769

Filed: June 27, 2003

For: Nonplanar Semiconductor Device with  
Partially or Fully Wrapped Around Gate  
Electrode and Methods of Fabrication

Examiner: Unassigned

Art Unit: 2812

Mail Stop Amendment  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

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Sir:

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to MS: Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on January 30, 2006  
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Dianne Neathery

(Typed or printed name of person mailing correspondence)

Dianne Neathery

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Pursuant to 37 C.F.R. § 1.97, the submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made and is not to be construed as an admission that the information cited in this statement is material to patentability.

Pursuant to 37 C.F.R. § 1.97, this Information Disclosure Statement is being submitted under one of the following (as indicated by an "X" to the left of the appropriate paragraph):


- X   37 C.F.R. §1.97(b).
- 37 C.F.R. §1.97(c). If so, then enclosed with this Information Disclosure Statement is one of the following:
- A statement pursuant to 37 C.F.R. §1.97(e) or
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If there are any additional charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: January 30, 2006

  
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# INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet

1

of

2

**Complete if Known**

Application Number	10/607,769
Filing Date	June 27, 2003
First Named Inventor:	Scott A. Hareland, et al.
Art Unit	2812
Examiner Name	Unassigned
Attorney Docket No.:	42P15685

**U.S. PATENT DOCUMENTS**

Examiner Initials*	Cite No. <sup>1</sup>	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code <sup>2</sup> (if known)				
		US-	6,475,890 B1	11-05-2002	Yu.	
		US-	2004/0227187	11-18-2004	Cheng et al.	Fig. 9B-10C
		US-	5,124,777	06-23-1992	Lee, Sangin	
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		US-	6,611,029 B1	08-26-2003	Ahmed et al.	
		US-				
		US-				

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				Application Number	10/607,769
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				Examiner Name	Unassigned
Sheet	2	of	2	Attorney Docket No.:	42P15685

FOREIGN PATENT DOCUMENTS								
Examiner Initials*	Cite No. <sup>1</sup>	Foreign Patent Document			Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>2</sup>
		Country Code <sup>3</sup>	Number <sup>4</sup>	Kind Code <sup>5</sup> (if known)				
		EP	1 566 844 A2		08-24-2005	Samsung Electronics Co.		

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T <sup>2</sup>
		International Search Report PCT/US2005/000947, Int'l. filing date January 10, 2005, mailed May 3, 2005 (7 pages).	
		T. Park et al., "Fabrication of Body-Tied FinFETs (Omega MOSFETS) Using Bulk Si Wafers", 2003 Symposia on VLSI Technology Digest of Technical Papers, June 2003, pages 135-136.	

Examiner Signature		Date Considered	
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